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Amendments To The Claims

The following list of the claims replaces all prior versions and lists of the claims in this application.

1. (Previously presented) A method of forming a semiconductor device on a semiconductor substrate, comprising the steps of:

forming a high dielectric constant (high k) gate dielectric layer on said semiconductor substrate, said gate dielectric layer having a dielectric constant greater than the dielectric constant of silicon oxide;

forming a conductive gate structure on a first area of said gate dielectric layer;

forming first insulator spacers on the sides of said conductive gate structure with the procedure used to form said first insulator spacers also removing a second area of said gate dielectric layer, wherein said second area of said gate dielectric layer is not covered by said conductive gate structure or by said first insulator spacers;

forming a first doped region in an area of said semiconductor substrate not covered by said conductive gate structure or by said first insulator spacers;

forming second insulator spacers on the sides of said first insulator spacers; and

forming a second doped region in an area of said semiconductor substrate not covered by said conductive gate structure, not covered by said first insulator spacers, and not covered by said second insulator spacers.

2. (Previously presented) The method of claim 1, wherein said gate dielectric layer is comprised of a layer selected from the group consisting of silicon nitride, tantalum oxide, silicon oxynitride, hafnium oxide, zirconium oxide, and aluminum oxide.

3. (Original) The method of claim 1, wherein the thickness of said gate dielectric layer is between about 10 to 200 Angstroms.

4. (Canceled).

5. (Original) The method of claim 1, wherein said conductive gate structure is comprised of doped polysilicon, at a thickness between about 300 to 3000 Angstroms.

6. (Original) The method of claim 1, wherein said conductive gate structure is comprised of metal silicide such as tungsten silicide.

7. (Original) The method of claim 1, wherein said first insulator spacers are comprised of silicon oxide, at a thickness between about 10 to 300 Angstroms.

8. (Original) The method of claim 1, wherein said first insulator spacers are comprised of silicon nitride, at a thickness between about 30 to 400 Angstroms.

9. (Previously presented) The method of claim 1, wherein the procedure used to define said first insulator spacers on sides of said conductive gate structure, and to remove exposed portions of said gate dielectric layer, is an anisotropic RIE procedure performed using Ar/CF_4 as a selective etchant for said first insulator spacers and for said gate dielectric layer.

10. (Currently amended) A method of forming a semiconductor device on a semiconductor substrate featuring a high dielectric constant (high k) gate insulator layer, comprising the steps of:

forming said high k gate insulator layer on said semiconductor substrate, said high k gate insulator layer having a dielectric constant greater than the dielectric constant of silicon oxide;

forming a conductive gate structure overlying a first area of said high k gate insulator layer;

depositing ~~an~~ a further insulator layer;

performing a dry etch procedure to first define first insulator spacers on the sides of said conductive gate structure via etching of said further insulator layer, and then to remove exposed portions of said high k gate ~~dielectric~~ insulator layer, wherein said exposed portions of said high k gate insulator layer are portions not covered by said conductive gate structure or by said first insulator spacers;

forming a lightly doped source/drain region in an area of said semiconductor substrate not covered by said conductive gate structure or by said first insulator spacers;

forming second insulator spacers on the sides of said first insulator spacers; and

forming a heavily doped source/drain region in an area of said semiconductor substrate not covered by said conductive gate structure, not covered by said first insulator spacers, and not covered by said second insulator spacers.

11. (Previously presented) The method of claim 10, wherein said high k gate insulator layer is selected from the group consisting of silicon nitride, tantalum oxide, silicon oxynitride, zirconium oxide, hafnium oxide, and aluminum oxide.

12. (Original) The method of claim 10, wherein the thickness of said high k gate insulator layer is between about 10 to 200 Angstroms.

13. (Canceled).

14. (Original) The method of claim 10, wherein said conductive gate structure is comprised of doped polysilicon, at a thickness between about 300 to 3000 Angstroms.

15. (Original) The method of claim 10, wherein said conductive gate structure is comprised of tungsten silicide.

16. (Currently amended) The method of claim 10, wherein said further insulator layer is selected from the group consisting of silicon oxide, silicon nitride, or silicon oxynitride.

17. (Currently amended) The method of claim 10, wherein the thickness of said further insulator layer is between about 30 to 500 Angstroms.

18. (Currently amended) The method of claim 10, wherein the procedure used to both define said first insulator spacers on sides of said conductive gate structure, and to remove exposed portions of said high k gate insulator layer, is an anisotropic RIE procedure performed using Ar/CF_4 as a selective etchant for said further insulator layer and for said high k gate insulator.

Claims 19-28 (Canceled).